

## AMENDMENTS TO THE CLAIMS

Please amend claim 14 as set forth below:

- 1 1. (original) A digital signal processor, comprising:
  - 2 a content addressable memory (CAM) array having a plurality of rows of CAM
  - 3 cells;
  - 4 an array of storage elements having a plurality of rows of the storage elements
  - 5 coupled to the CAM array, each row of storage elements to store a number corresponding
  - 6 to a data word stored in one of the rows of the CAM cells; and
- 7 priority logic coupled to the array of storage elements, the priority logic to provide
- 8 to a plurality of priority signal lines an indication of a location of a particular number in
- 9 the array of storage elements, wherein the priority logic comprises:
  - 10 a first plurality of compare circuits, each compare circuit coupled to one of
  - 11 the storage elements in the array of storage elements, and each compare circuit
  - 12 having a first input coupled to a storage element, a second input coupled to a
  - 13 match line, and an input/output line coupled to one of the plurality of priority
  - 14 signal lines; and
  - 15 a delay circuit coupled to each of the first plurality of compare circuits.
- 1 2. (original) The digital signal processor of claim 1, wherein the delay circuit
- 2 comprises a multiple tap delay circuit.
- 1 3. (original) The digital signal processor of claim 1, wherein the delay circuit
- 2 comprises a plurality of delay elements, each of the plurality of delay elements coupled to
- 3 one of the plurality of compare circuits.
- 1 4. (original) The digital signal processor of claim 3, wherein each of the delay
- 2 elements is programmable.
- 1 5. (original) The digital signal processor of claim 1, wherein each of the compare
- 2 circuits comprise a first transistor having a drain coupled to a corresponding priority

3 signal line and having a gate coupled to a corresponding storage element.

1 6. (original) The digital signal processor of claim 5, wherein the gate of the first  
2 transistor is coupled to the delay circuit through one or more logic gates.

1 7. (original) The digital signal processor of claim 6, wherein the delay circuit  
2 comprises a plurality of delay elements, each of the plurality of delay elements having an  
3 output coupled to one of the plurality of compare circuits.

1 8. (original) The digital signal processor of claim 7, wherein the one or more logic  
2 gates comprise a NAND gate having a first input coupled to a corresponding match line  
3 and a having a second input coupled to a corresponding output of one of the delay  
4 elements.

1 9. (original) The digital signal processor of claim 8, wherein the NAND gate has an  
2 output and wherein the one or more logic gates further comprise a NOR gate having a  
3 first input coupled the output of the NAND gate, and wherein the NOR gate has an output  
4 coupled to the gate of the first transistor.

1 10. (original) The digital signal processor of claim 1, further comprising:  
2 a policy statement table for storing a plurality of policy statements; and  
3 a priority index table for storing a plurality of priority numbers, each priority  
4 number associated with a corresponding policy statement and indicating the priority of the  
5 corresponding policy statement relative to the other policy statements, wherein the priority  
6 index table comprises the priority logic coupled to the policy statement table, wherein the  
7 priority logic provides the most significant priority number to a plurality of priority signal  
8 lines.

1 11. (original) The digital signal processor of claim 1, wherein the first plurality of  
2 compare circuits are coupled in a sequence, each of compare circuit having a third input  
3 coupled to a preceding compare circuit in the sequence.

1 12. (original) The digital signal processor of claim 11, wherein each of the compare  
2 circuits comprise a first transistor having a drain coupled to a corresponding priority  
3 signal line and having a gate coupled to a corresponding storage element, wherein the  
4 gate of the first transistor is coupled to the delay circuit through one or more logic gates.

1 13. (original) The digital signal processor of claim 12, wherein the third input of the  
2 compare circuit is coupled to the one or more logic gates.

1 14. (currently amended) The digital signal processor of claim 13, wherein the one or  
2 more logic gates comprise a first NOR gate having a first input ~~coupled to the third input~~  
3 coupled to the third input of the compare circuit, the first NOR gate having an output coupled to  
4 the gate of the first transistor.

1 15. (original) The digital signal processor of claim 14, wherein each of the compare  
2 circuits further comprises a second NOR gate having an input coupled to the gate of the  
3 first transistor, the second NOR gate having an output coupled to the first NOR gate of a  
4 succeeding compare circuit in the sequence.

1 16. (previously presented) A method of operating a digital signal processor,  
2 comprising:

3 outputting a first priority number signal on a priority line coupled to a first  
4 column of compare circuits, the first priority number signal having one of at least two  
5 logical signal levels based, at least in part, on a comparison of priority number bits stored  
6 within a first column of priority number storage elements coupled to the first column of  
7 compare circuits; and

8 concurrently de-asserting a match line in the first column of compare circuits and  
9 outputting a second priority number signal on a next priority line coupled to a second  
10 column of compare circuits, the second priority number signal having one of the at least  
11 two logical signal levels based, in part, on a comparison of priority number bits stored  
12 within a second column of priority number storage elements coupled to the second  
13 column of compare circuits.

1 17. (original) The method of claim 16, further comprising de-asserting a match line  
2 in the second column of compare circuits.

1 18. (previously presented) A digital signal processor, comprising:  
2 means for outputting a first priority number signal on a priority line coupled to a  
3 first column of compare circuits, the first priority number signal having one of at least  
4 two logical signal levels based, at least in part, on a comparison of priority number bits  
5 stored within a first column of priority number storage elements coupled to the first  
6 column of compare circuits; and  
7 means for concurrently de-asserting a match line in the first column of compare  
8 circuits and outputting a second priority number signal on a next priority line coupled to a  
9 second column of compare circuits, the second priority number signal having one of the  
10 at least two logical signal levels based, in part, on a comparison of priority number bits  
11 stored within a second column of priority number storage elements coupled to the second  
12 column of compare circuits.

1 19. (original) The digital signal processor of claim 17, further comprising means for  
2 de-asserting a match line in the second column of compare circuits.